15. (New) The integrated circuit of claim 14 wherein the second enable control input is coupled to a logic element.

16. (New) A programmable logic integrated circuit comprising:

a plurality of logic array blocks;

a programmable interconnect bus, programmably coupled to the plurality of logic array blocks;

a tristate bus comprising a plurality of conductors; and

a plurality of tristate devices, coupled between the plurality of logic array blocks and one conductor of the tristate bus, wherein the plurality of tristate devices couple and decouple the logic array blocks to the one conductor of the tristate bus, and at least one of the tristate devices comprises:

a data input;

an enable input;

a first driver transistor, coupled between a first potential source and an output node;

a second driver transistor, coupled between the output node and a second potential source;

a first predriver comprising:

a first transistor, coupled between the first potential source and a control electrode of the first driver transistor, having a control electrode coupled to a complement of the enable input;

a second transistor, coupled between the control electrode of the first driver transistor and control electrode of the second driver transistor, having a control electrode coupled to the complement of the enable input; and

a third transistor, coupled between the control electrode of the second driver transistor and the second potential source, having a control electrode coupled to the enable input; and

a second predriver comprising:

a first transistor, coupled between the first potential source and the control electrode of the first driver transistor, having a control electrode coupled to the data input;

an enable input;

a first driver transistor, coupled between a first potential source and an output node;

a second driver transistor, coupled between the output node and a second potential source;

a first predriver comprising:

a first transistor, coupled between the first potential source and a control electrode of the first driver transistor, having a control electrode coupled to a complement of the enable input;

a second transistor, coupled between the control electrode of the first driver transistor and control electrode of the second driver transistor, having a control electrode coupled to the complement of the enable input; and

a third transistor, coupled between the control electrode of the second driver transistor and the second potential source, having a control electrode coupled to the enable input; and

a second predriver comprising:

a first transistor, coupled between the first potential source and the control electrode of the first driver transistor, having a control electrode coupled to the data input;

a second transistor, coupled between the control electrode of the first driver transistor and the control electrode of the second driver transistor, having a control electrode coupled to the enable input; and

a third transistor, coupled between the control electrode of the second driver transistor and the second potential source, having a control electrode coupled to the data input,

wherein the enable input is controlled by way of a logic element.

12. (New) The integrated circuit of claim 11 wherein the output node is coupled to a programmable interconnect structure.

13. (New) The integrated circuit of claim 11 further comprising first and second enable control inputs logically coupled to the enable input.

14. (New) The integrated circuit of claim 13 wherein the first enable control input is coupled to a programmable memory cell.

a second transistor, coupled between the control electrode of the first driver transistor and the control electrode of the second driver transistor, having a control electrode coupled to the enable input; and

a third transistor, coupled between the control electrode of the second driver transistor and the second potential source, having a control electrode coupled to the data input.

17. (New) The integrated circuit of claim 16 wherein the plurality of tristate devices couple and decouple the logic array blocks to the one conductor of the tristate bus by way of a logic signal from a logic array block.

18. (New) The integrated circuit of claim 16 further comprising:

a plurality of OE generation circuits, coupled to the plurality of tristate devices, the plurality of OE generation circuits controlling the plurality of tristate devices.

19. (New) The integrated circuit of claim 18 wherein a logic array block programmably couples to drive the plurality of OE generation circuits.

20. (New) The integrated circuit of claim 16 further comprising:

a further tristate device, coupled between the tristate bus and the programmable interconnect bus, for driving signals between the tristate bus and programmable interconnect bus.

21. (New) A programmable logic integrated circuit comprising:

a programmable interconnect bus; and

a logic array block, comprising:

a plurality of logic elements configurable to perform logical functions;

a plurality of tristate devices, coupled between the plurality of logic elements and the programmable interconnect bus; and

tristate control logic to dynamically control states of the plurality of tristate devices, wherein at least one of the tristate devices comprises:

a data input;

an enable input;

a first driver transistor, coupled between a first potential source and an output node;

a second driver transistor, coupled between the output node and a second potential source;

a first predriver comprising:

a first transistor, coupled between the first potential source and a control electrode of the first driver transistor, having a control electrode coupled to a complement of the enable input;

a second transistor, coupled between the control electrode of the first driver transistor and control electrode of the second driver transistor, having a control electrode coupled to the complement of the enable input; and

a third transistor, coupled between the control electrode of the second driver transistor and the second potential source, having a control electrode coupled to the enable input; and

a second predriver comprising:

a first transistor, coupled between the first potential source and the control electrode of the first driver transistor, having a control electrode coupled to the data input;

a second transistor, coupled between the control electrode of the first driver transistor and the control electrode of the second driver transistor, having a control electrode coupled to the enable input; and

a third transistor, coupled between the control electrode of the second driver transistor and the second potential source, having a control electrode coupled to the data input.

22. (New) The integrated circuit of claim 21 wherein the plurality of tristate devices are programmably enabled to couple the plurality of logic elements to the programmable interconnect bus.

23. (New) The integrated circuit of claim 21 wherein the tristate control logic is programmably coupled to signals on the programmable interconnect bus for controlling the states of the plurality of tristate devices.

24. (New) The integrated circuit of claim 21 wherein one of the plurality of logic elements is coupled through one of the plurality of tristate devices through the programmable interconnect bus to another one of the plurality of logic elements.

25. (New) A programmable logic integrated circuit comprising:

a tristate bus;

a plurality of source logic array blocks;

a first plurality of tristate devices coupling the source logic array blocks to the tristate bus; and

a destination logic array block coupled to receive signals from the tristate bus, wherein at least one of the tristate devices comprises:

a data input;

an enable input;

a first driver transistor, coupled between a first potential source and an output node;

a second driver transistor, coupled between the output node and a second potential source;

a first predriver comprising:

a first transistor, coupled between the first potential source and a control electrode of the first driver transistor, having a control electrode coupled to a complement of the enable input;

a second transistor, coupled between the control electrode of the first driver transistor and control electrode of the second driver transistor, having a control electrode coupled to the complement of the enable input; and

a third transistor, coupled between the control electrode of the second driver transistor and the second potential source, having a control electrode coupled to the enable input; and

a second predriver comprising:

a first transistor, coupled between the first potential source and the control electrode of the first driver transistor, having a control electrode coupled to the data input;

a second transistor, coupled between the control electrode of the first driver transistor and the control electrode of the second driver transistor, having a control electrode coupled to the enable input; and

a third transistor, coupled between the control electrode of the second driver transistor and the second potential source, having a control electrode coupled to the data input.

26. (New) The integrated circuit of claim 25 wherein signals on the tristate bus cannot be coupled to an input of the destination logic array block without passing through another bus.

27. (New) The integrated circuit of claim 25 wherein the tristate bus cannot be directly coupled to an input of the destination logic array block.

28. (New) The integrated circuit of claim 25 further comprising:

a second plurality of tristate devices to buffer signal from the tristate bus to inputs of the destination logic array block.

29. (New) The integrated circuit of claim 28 wherein the states of the first plurality of tristate devices are logically controlled and may be dynamically changed.

30. (New) The integrated circuit of claim 29 wherein the states of the second plurality of tristate devices are logically controlled and may be dynamically changed.

31. (New) The integrated circuit of claim 25 wherein a source logic array block comprises:

a plurality of logic elements, each coupling to a different conductor of the tristate bus.

32. (New) The integrated circuit of claim 25 wherein for each source logic array block, a logic element in a first position is coupled to a first conductor of the tristate bus, and a logic element in a second position is coupled to a second conductor of the tristate bus.

33. (New) A method of multiplexing signals onto an interconnect line comprising:

enabling a first tristate driver having an input coupled to a first logic element and an output coupled to the interconnect line, such that a signal is driven from the first logic element onto the interconnect line using the first tristate driver;

dynamically tristating the first tristate driver; and

dynamically enabling a second tristate driver having an input coupled to a second logic element and an output coupled to the interconnect line, such that a signal is driven from the second logic element onto the interconnect line using the second tristate driver.

34. (New) The method of claim 33 further comprising:
dynamically tristating the second tristate driver.

35. (New) The method of claim 33 wherein the first tristate driver is dynamically tristated without reconfiguring a memory cell.

36. (New) The method of claim 35 wherein the second tristate driver is dynamically enabled without reconfiguring a memory cell.

37. (New) The method of claim 33 wherein the first tristate driver is dynamically tristated using a first tristate control circuit.

38. (New) The method of claim 37 wherein the second tristate driver is dynamically enabled using a second tristate control circuit.

39. (New) The method of claim 33 wherein the first tristate driver is dynamically tristated using a third logic element.

40. (New) The method of claim 39 wherein the second tristate driver is dynamically enabled using a fourth logic element.

41. (New) A method of allowing a first logic element to couple to an interconnect line comprising:
permitting a programmable memory cell to control a first enable input of a tristate driver; and
permitting an output of a second logic element to dynamically control a second enable input of the tristate driver, such that when the output of the second logic element is a first state, the first logic element is coupled to the interconnect line.

42. (New) The method of claim 41 wherein the interconnect line is a vertical programmable conductor.

43. (New) The method of claim 41 wherein the interconnect line is a conductor in a tristate bus.

44. (New) A method of coupling a first logic element to an interconnect line comprising:

programming a memory cell coupled to a first enable input of a tristate driver; and

driving a second logic element coupled to a second enable input of the tristate driver, such that when the second logic element is in a first state, the first logic element is coupled to the interconnect line.

45. (New) The method of claim 44 further comprising:

driving the second logic element coupled to the second enable input of the tristate driver, such that when the second logic element is in a second state, the first logic element is not coupled to the interconnect line.

46. (New) The method of claim 45 wherein the interconnect line is a vertical programmable conductor.

47. (New) The method of claim 45 wherein the interconnect line is a conductor in a tristate bus.

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48. (New) A programmable logic integrated circuit comprising:

a programmable interconnect bus;

a plurality of logic elements configurable to perform logical functions;

a plurality of tristate devices coupled between the plurality of logic elements and the programmable interconnect bus;

a plurality of programmable memory cells coupled to the plurality of tristate devices to programmably enable and programmably tristate the plurality of tristate devices; and

tristate control logic coupled to the plurality of tristate devices to dynamically enable and dynamically tristate the plurality of tristate devices.

49. (New) The integrated circuit of claim 48 wherein the tristate control logic is programmably coupled to signals on the programmable interconnect bus for controlling the states of the plurality of tristate devices.

50. (New) The integrated circuit of claim 48 wherein one of the plurality of logic elements is coupled through one of the plurality of tristate devices through the programmable interconnect bus to another one of the plurality of logic elements.

51. (New) The integrated circuit of claim 48 wherein the tristate control logic comprises a logic element.

52. (New) A programmable logic integrated circuit comprising:

a first logic element having a first output;

a tristate driver having a first enable input, a second enable input, a second output, and an input coupled to the first output;

a programmable memory cell coupled to the first enable input;

a second logic element coupled to the second enable input; and

an interconnect line coupled to the second output,

wherein the second logic element may dynamically tristate and dynamically enable the tristate driver.

53. (New) The integrated circuit of claim 52 wherein the interconnect line is a vertical conductor.

54. (New) The integrated circuit of claim 52 wherein the interconnect line is in a tristate bus.